IN THE CLAIMS

A clean set of all pending claims is submitted, consolidating all previous versions of pending claims. If changes have been made to the previous version of the claims by the current response, the clean set is followed by a marked-up version indicating the changes made (see 37 CFR 1.121(c)(3)).

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1. (AMENDED) An apparatus comprising:

a first circuit configured to wake up a second circuit in response to an input signal, wherein said input signal comprises a programmable delay value.

2. The apparatus according to claim 1, wherein said input signal comprises a user programmable signal.

3. The apparatus according to claim 1, wherein said input signal comprises a multi-bit signal.

4. (AMENDED) The apparatus according to claim 1, wherein said programmable delay value is determined by said apparatus in response to one or more firmware instructions.

5. (AMENDED) The apparatus according to claim 1, wherein said programmable delay value comprises a wake-up delay timing value.

6. (AMENDED) The apparatus according to claim 1, wherein said first circuit comprises:

a delay circuit configured to present a first delay signal; and

a select circuit configured to present a second delay signal in response to said first delay signal and said input signal, wherein said second delay signal is configured to wake up said second circuit.

7. The apparatus according to claim 6, wherein said input signal is configured to control a programmable delay of said second delay signal.

8. (AMENDED) The apparatus according to claim 7, wherein said programmable delay comprises a multiple of a delay of said first delay signal.

9. (AMENDED) The apparatus according to claim 6, wherein said select circuit is further configured to select one of

a plurality of third delay signals in response to said input signal.

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10. The apparatus according to claim 6, wherein said select circuit comprises:

a divider circuit configured to present one or more divided signals in response to said first delay signal; and

a multiplexer configured to present said second delay signal in response to said one or more divided signals and said input signal.

11. (AMENDED) The apparatus according to claim 6, wherein said select circuit comprises a counter configured to generate said second delay signal in response to said input signal and said first delay signal.

12. (AMENDED) The apparatus according to claim 6, wherein said delay circuit is further configured to present said first delay signal in response to an enable signal.

13. The apparatus according to claim 1, wherein said input signal is generated in response to a device selected from the group consisting of input pins, data pins, microprocessor code, and firmware.

14. (AMENDED) An apparatus comprising:

a first circuit configured to operate in a sleep mode and a wake-up mode; and

a second circuit configured to control switching of said first circuit from said sleep mode to said wake-up mode after a programmable period of time.

15. (AMENDED) A method for wake-up timing comprising the steps of:

(A) receiving an input signal; and

(B) waking-up a circuit after a delay time determined in response to said input signal, wherein said input signal comprises a programmable delay value.

16. (AMENDED) The method according to claim 15, wherein said input signal comprises a user programmable signal and said programmable delay value comprises a wake-up timing value.

17. (AMENDED) The method according to claim 15, wherein said programmable delay value is determined in response to execution of one or more computer executable instructions stored in a computer readable medium.

18. (AMENDED) The method according to claim 15, wherein step (B) further comprises the sub-steps of:

(B-1) presenting a first delay signal; and

(B-2) presenting a second delay signal in response to said first delay signal and said programmable delay value, wherein said second delay signal is configured to wake-up said circuit.

19. (AMENDED) The method according to claim 18, wherein step (B) further comprises the sub-step of:

(B-3) controlling a programmable delay of said second delay signal in response to said programmable delay value.

20. (AMENDED) The method according to claim 15, further comprising the step of:

(C) generating said input signal in response to a comparison of a measured wake-up delay to a predetermined wake-up delay.

Please add the following new claims:

21. (NEW) The apparatus according to claim 1, wherein said first and second circuits are implemented on a single integrated circuit.

22. (NEW) The apparatus according to claim 1, wherein (i) said first circuit is configured to periodically wake up said second circuit and (ii) a sleep period of said second circuit is determined by said programmable delay value.

23. (NEW) The apparatus according to claim 1, wherein said second circuit is configured to generate said input signal.

24. (NEW) The method according to claim 15, further comprising:

setting an initial value for said programmable delay value;

enabling a wake-up delay timer configured to generate a wake-up signal in response to said programmable delay value;

measuring a delay time of said wake-up timer; and

adjusting said programmable delay value in response to said measured delay time.

25. (NEW) The apparatus according to claim 14, wherein said second circuit is configured to determine said programmable period of time in response to an input signal comprising a programmable delay value.